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(54) Packet transfer control arrangement and related method.

(57) The packet transfer control arrangement ensures that an information packet transferred from an input to an output of a packet switching network is available in correct form at that output. It includes copying means (SE11/SEmn) located at the input of the network to make copies of the packet to be transferred, routing means (HA11/HAmn; SE11/SEmn) to transfer these copies independently from each other and possibly over at least partly distinct paths from an input to an output of the network and filtering modules (F11/Fmn) to filter out one of the copies at the output of the network.

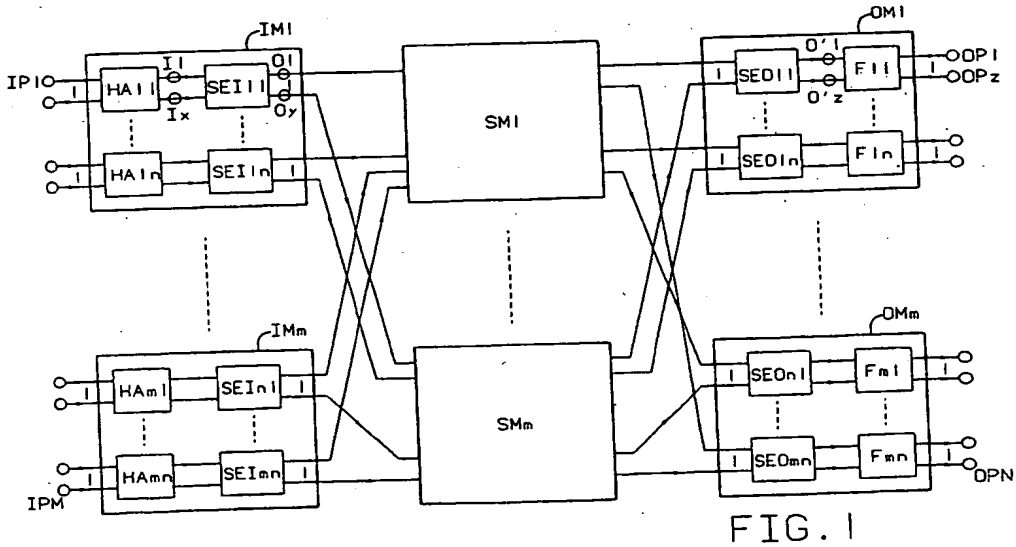

FIG. 1

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The present invention relates to a packet transfer control arrangement to ensure that an information packet transferred from an input to an output of a packet switching network is available in correct form at said output.

Such an arrangement is already known in the art, e.g. from the article "A flexible network architecture for the introduction of ATM" by D.G. Fisher et al, Proceedings of the XIIIth International Switching Symposium, 1990, Stockholm, Volume II, pp. 35-44. In this known arrangement the switching network includes duplicated network modules called planes and for each packet to be transferred it establishes more than one path over the planes and between two ports of the network. In this way a relatively high probability for a transferred packet to reach the output port is ensured.

Such a duplication of the network elements of course results in a corresponding increase of the network costs.

An object of the invention is to provide an arrangement of the above type but requiring less redundancy in the switching network.

This object is achieved due to the fact that said arrangement includes :

- copying means at said input to make at least two copies of said information packet,
- means to transfer said copies independently from each other over said packet switching network to said output; and
- a filtering module at said output to filter out one copy of said copies and apply it to said output.

The probability for two or more copies of a packet to get lost or corrupted is substantially lower than it is for one copy.

Thus receipt of packets in a correct form is ensured without the need for increasing redundancy.

An additional feature of the invention is that said arrangement also includes routing means which are associated to said copying means and include in said copies routing information to route said copies through said switching network over at least partly separate paths.

In this way the possibility of packet loss or corruption is even more reduced.

The invention also relates to a filtering module for filtering one copy of a packet of information out of at least two copies of said packet, said copies being transferred from an input to an output of a packet switching network.

This module is characterized in that it includes:

- a plurality of memory modules;
- selection means to receive said copies, to register the receipt of a first acceptable copy of said copies at a selected location of a selected one of said memory modules and to discard any other copy;
- clearing means to clear said selected location after a predetermined time interval starting at the receipt of a first one of said copies, said selected location being then again available;

said plurality of memory modules being determined at least by the transfer time of said copies over said network and the time needed by said clearing means to clear said selected location.

By adapting the number of memory modules to the speed of the packet transfer the filtering module is able to be used with any transmission speed. The higher the speed, i.e. the lower the transfer time or delay of the packets, the more memory modules are needed to give the clearing means the time to clear one module while the selection means use one or more other modules. The clearing means evaluate the instant of clearing of a memory module and the identity of the modules to be used in the meantime by the selection means is determined by the latter in function of the transfer delay of the packets and the time needed by the clearing means to clear a module.

The invention also relates to a method for ensuring that an information packet transferred from an input to an output of a packet switching network is available in correct form at said output.

Such a method is also described in the above mentioned article and has the same drawback as the related known packet transfer control arrangement. It indeed needs duplicated network elements giving rise to an increased network cost.

An additional object of the invention is to provide a method of the above type but without the drawback mentioned.

This object is achieved due to the fact that said method includes, for each packet to be transferred, the steps of :

- making at least two copies of said packet;
- transferring said copies over said network to said output; and
- filtering at said output one acceptable copy out of said copies.

By copying the packets and transferring the copies to the same mentioned output the possibility of loss and/or corruption of packets is reduced as explained above without a need for increasing the number of network elements.

An additional feature of the above method is that said copies are transferred over said network in such a way that they follow paths which are at least partly distinct.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

Fig. 1 is a block diagram of a packet switching network with and associated packet transfer control arrangement according to the invention;

Fig. 2 represents in more detail the switching element SEI11 of Fig. 1;

Fig. 3 shows the filtering circuit F11 of Fig. 1 in more detail;

Fig. 4 is a time diagram related to the control of the memory unit MU of Fig. 3.

The packet switching network represented in Fig. 1 is a multiple path, self routing network of the type disclosed in the not yet published European patent application 90200593.3, and has a packet transfer control arrangement associated to it. It is used to transfer packets of information from any of its M input ports IP1 to IPM to one or more of its N output ports OP1 to OPN.

The network is built-up by means of m input modules IM1 to IMm, m switching modules SM1 to SMm and m output modules OM1 to OMm, all interconnected as shown by bundles of external links.

The input modules IM1 to IMm each include a number of header conversion modules and a number of switching elements. For example, IM1 includes n header conversion modules HA11 to HA1n which are connected to respective ones of n switching elements SEI11 to SEI1n via sets of links. For instance, HA11 is coupled to the x inputs I1 to Ix of SEI11 by means of the set of x links I1 to Ix and SEI11 has y output terminals O1 to Oy connected to like named external links

The values M, N, m, n, x, y, are determined by the size of the network. Typical values are x = 8, y = 8, n = 16, m = 16 which results in M = N = 2048.

The switching modules SM1 to SMm are constituted of a plurality of interconnected switching elements (not shown) identical to SEI11. Two variants of such switching modules are disclosed in the above mentioned European patent application and these modules are therefore not described in detail.

The output modules OM1 to OMm each include a number of switching elements and a number of filtering modules. For example, OM1 includes n switching elements SEO11 to SEO1n which are connected to respective ones of n filtering modules F11 to F1n via sets of links. For instance, SEO11 is coupled to z inputs O'1 to O'z of F11 by means of the set of z links O'1 to O'z and F11 has z output terminals OP1 to OPz connected to like named external links. A typical value of z is 8.

Each of the information packets arriving at the input ports of the network comprises a header and an information part generally called payload part, the header including routing information and information concerning the required number of copies to be made.

Each of the header conversion modules, such as HA11, is able to analyse the header of a packet supplied to one of its inputs and to convert, by using a translation table (not shown), the information contained in the header of the packet to a predetermined code known by the switching elements included in the network and indicating to each of these switching elements the number of copies to be made and the address of the switching element output port to which each of these copies has to be transferred.

Each header conversion module additionally inserts in the header of the packet a packet identifier, more specifically a time stamp TSTP, and a connection identifier CI identifying the communication to which the packet belongs. The design of an header conversion module by a person skilled in the art is obvious from its functional description and is therefore not described in detail.

The switching elements of the network are all identical and are of a type such as disclosed in the published International patent application PCT/EP89/00942. One of them, namely SEI11, is represented in detail in Fig. 2. It has inputs I1 to Ix connected to respective data inputs of a multiplexer circuit MX through the cascade connection of a respective series-to-parallel converter circuit SP1/SPx and a respective latch circuit IL1/ILx. The selection input XI of the multiplexer MX is controlled by an input clock circuit XC and its data output is coupled to the data input CI of a RAM buffer memory BM.

The buffer memory BM further has a data output which is coupled to the data input of a demultiplexer DX whose selection input YI is controlled by an output clock circuit YC and whose data outputs are coupled to respective ones of the outputs 01/Oy via respective ones of parallel-to-series converter circuits PS1/PSy. The output clock circuit YC is such that the demultiplexer DX is able to successively connect its data input to its data outputs.

The buffer memory BM comprises a number of buffers or memory locations which are each able to store a single packet, and has an address input AC as well as a read/write selection input RW, these inputs being respectively coupled to like named outputs of a buffer memory management unit BMMU.

The switching element SEI11 further includes a routing logic RL whose input is coupled to the data output CI of the multiplexer MX. The routing logic RL is able to interprete information contained in the header of a packet and to then supply to the buffer memory management unit BMMU a control signal C which is function of this information. More par-

ticularly, the latter control signal C contains a set of addresses, of one or more of the outputs O1/Oy, to each of which a copy of the packet has to be transferred. This means that the number of addresses is equal to the number of these copies

The buffer memory management unit BMMU is coupled to the above mentioned selection inputs XI and YI of MX and DX respectively, and under control of the control signal C it manages the use of the buffers of the memory BM.

A more complete description of the switching element SEl11 may be found in the mentioned International patent application.

The above mentioned filtering modules F12 to Fmn shown in Fig. 1 are all identical to the module F11 represented in Fig. 3. The latter module includes a multiplexer circuit MUX1 with input terminals O'1 to O'z and with a selection input controlled by an input clock circuit MC under the control of which the multiplexer is able to successively connect its inputs to its data output. The latter is coupled to a data input of a header processing unit HPU which also has a control input C' to which a like named signal C' is applied from a memory unit MU.

This header processing unit HPU further has a data output connected to the input of a demultiplexer DMUX and three control outputs P, CI, TSTP on which like named signals are provided and which are connected to corresponding inputs of a second multiplexer circuit MUX2 and a control unit CU. HPU finally has a fourth control output S/R and a fifth control output S coupled to a set/reset circuit S/R and to the selection input S of the demultiplexer DMUX respectively.

MUX2 more precisely comprises three 2-to-1 multiplexers (MUX21, MUX22, MUX23) with a common selection input S'. The control outputs P, CI, TSTP of HPU are connected to a first input of respective ones of these 2-to-1 multiplexers. MUX2 has three outputs constituted by the outputs of the three 2-to-1 multiplexers and connected to an address input of the memory unit MU. The latter unit is controlled by the set/reset circuit S/R and is subdivided in a plurality of not shown storage units called pages.

The control unit CU has a control input to which the signal C' is applied and 3 data outputs each coupled to a second input of respective ones of the 2-to-1 multiplexers of the multiplexer MUX2, a first control output S' connected to the selection input S' of the multiplexer MUX2, and a second control output S/R' coupled to the set/reset circuit S/R.

The outputs OP1 to OPz of the demultiplexer DMUX constitute the outputs OP1 to OPz of the filtering module F11.

Reference is now made to Figs 1 to 3 for a description of the routing of a packet through the switching network and of the operation of the packet transfer control arrangement associated therewith.

An information packet arriving at one of the input ports of the switching network, e.g. IP1 of Fig. 1, is analyzed by the associated header conversion module HA11. As mentioned earlier, this module HA11 converts the information contained in the header of the packet into a code to be interpreted by the switching elements of the network through which the packet has to be routed.

The packet with converted header is for instance transferred to input terminal I1 of the switching element SE11 represented in Fig. 2. This packet is converted in the corresponding series-to-parallel convertor circuit SP1 of SE11 and from this convertor circuit SP1 the thus obtained parallel version of the packet is transferred to the corresponding latch circuit IL1. From there it is supplied to the multiplexer MX from which it is transferred, under control of the clock signal XI provided by XC at the selection input of MX, to the data input CI of the buffer memory BM and of the routing logic RL. By means of a local routing table the earlier mentioned code provided by the header assignment module HA11, is converted to a set of one or more addresses of the outputs O1/Oy to each of which a copy of the packet has to be sent, i.e. the number of output addresses corresponds to the number of copies to be made of the packet as mentioned earlier. This set of addresses is passed to the unit BMMU by means of the control signal C.

It has to be noted that the local routing table can be, and mostly is, different for the different switching elements of the network. The latter table is established based on the structure of the packet switching network and on the reliability of the switching elements of that network.

Under control of the above activated signal XI provided by XC the unit BMMU provides the address of a free buffer at the address input AC of the memory BM and applies an activated signal to the input RW thereof. As a consequence the packet at the data input CI of the buffer memory BM is written in that free buffer and the address thereof is made busy by the unit BMMU by adding it to a list of busy buffers. This list also contains for each buffer address the above set of output port addresses to which the buffered packet has to be sent.

During a read-out operation the clock signal YI provided by the clock circuit YC indicates to the unit BMMU to which one of its outputs and consequently to which output address the demultiplexer DX has to convey a packet applied to its input. BMMU then searches in its list of busy

buffers for a buffer whose contents have to be sent to the latter address and supplies the address of this buffer to the address input AC of the buffer memory BM. It also applies a deactivated signal to the input R/W. As a consequence the packet contained in the corresponding buffer is read-out and transferred to the data output of the buffer memory BM. From there the packet is supplied by the demultiplexer DX to the output thereof which is indicated by the selection signal YC. Afterwards it is applied to the input of the corresponding parallel-to-series conversion circuit PS1/y by which it is provided at the corresponding output O1/Oy.

The output port address to which the copy was routed is then deleted by the unit BMMU from the above mentioned set of output port addresses linked to the considered buffer address of the busy buffer list. The buffer address itself remains in the latter list as long as there are output port addresses linked to it.

From the above it follows that in each switch element of the network means, more specifically BMMU and BM, are provided to make copies of a packet which has to be transferred and that the header conversion modules HA11 to HAmn constitute routing means which insert routing information in the headers of the copies to route them through the network via separate or distinct paths.

In this way a relatively safe transfer of the packet over the network is ensured since the probability of simultaneous loss or corruption of two or more packets is obviously much lower than the probability of loss or corruption of a single one.

It has to be noted that the paths followed by the copies of a packet do not necessarily have to be completely separate or distinct. For instance, if the probability of packet loss is relatively high on a well known critical part of a path, whereas it is low on the rest of the path, it is sufficient for the copies of this packet to follow a different route only for the critical path part. The copies can even be sent over the network without indication in their header of a predetermined path, thereby relying on the fact that the probability that two copies will follow the same path is relatively low. In that case the header of the packet only contains an indication of the number of copies to be made and of their destination address.

It has also to be noted that the above mentioned probability decreases with the number of copies until a minimum is reached. Beyond this minimum there is an increase of the possibility for loss of packets due to overload caused by the relatively high number of copies. To avoid this overload, a restricted redundancy of network modules might be necessary. However, this redundancy can be dimensioned according to the expected ratio of high quality connections, i.e. based on multiple connections, versus low quality connections i.e. based on single connections.

A more detailed description of the working of the switching elements of the network may be found in the earlier mentioned international patent application PCT/EP89/000942.

When the copies of a packet have been routed through the network, in the way described above, they consecutively appear at an input of a filtering module, e.g. input O'1 of F11, which is determined by the routing information specified in the header of the original packet.

Filtering of these copies, i.e. the extraction of a single copy, is explained hereafter by making reference to Fig. 3.

By the multiplexer MUX1 and under the control of the clock circuit MC all copies are consecutively applied to the header processing unit HPU. The latter unit analyses the header information of each copy received and extracts from it the earlier mentioned time stamp TSTP and the connection identifier CI and provides them together with a page number P at its respective control outputs TSTP, CI and P. How this page number is determined will be explained later. The page number P, the time stap TSTP and the connection identifier CI are applied to the address inputs of the digital memory unit MU via MUX2. Together they constitute a memory address. How the selection input of MUX2 is controlled will also be explained later.

The header processing unit HPU generates the earlier mentioned fourth signal S/R and applies it to the set/reset circuit S/R to indicate to the memory unit MU that on a page number P supplied on its input P and at a sub-address thereof, derived from the identifier CI and the time stamp TSTP, supplied at its inputs CI and TSTP respectively a value 1 has to be written in MU. If the current value stored at that location is 0, indicating that no copy of the packet with identifier CI and time stamp TSTP has been received yet and that the received copy is the first one of a set of copies of the latter packet, then a deactivated signal C' is generated by the memory unit MU. If the latter value is already 1, this means that a copy with a header including a same packet identifier TSTP and a same connection identifier CI, i.e. a copy of the same packet, has already been stored and that the copy just received is not the first one and must therefore be discarded. This fact is indicated by an activated signal C' generated by the memory unit MU. The signal C' is applied to the input C' of the header processing HPU which passes the copy to the demultiplexer DMUX or discards it depending on the signal C' being deactivated or activated respectively. The header processing unit HPU constitutes selection means which for each copy of a packet, received at its input, checks whether this copy is the first one and selects it for further processing if

this is the case. If not, the copy is discarded.

HPU controls the selection input of DMUX so that the latter passes the copy applied to its input to the one of the output ports OP1/z having the address contained in the header of the copy.

In this way a first copy of a packet is filtered out of a plurality of copies thereof by the filtering unit F11.

The control unit CU controls the clearing of the memory pages of MU. The instants and sequence of clearing these pages, as well as the value of the page number P generated by the header processing unit HPU, are determined by the transfer rate of the packets, more specifically the minimum and maximum transfer time of a packet through the network, by the time needed to clear a page and by the wrap-around value of the time stamp TSTP. The latter value is the maximum TSTP value after which an initial TSTP value is reused. The current TSTP value is obtained by incrementing a previous TSTP value with a predetermined value, starting from the mentioned initial value. How the above parameters are defined will be explained later.

The above time stamp TSTP, connection identifier CI and page P values are also passed to the control unit CU. At the instant of clearing an element of page P the control unit CU applies these values to the respective inputs of the 2-to-1 multiplexers of MUX2 and controls the selection input S' thereof so that these values are applied at the inputs of the memory unit MU. At the same time the control unit CU forces the set/reset circuit S/R to apply an activated reset signal to the control input of the memory unit MU. As a consequence the memory unit MU resets the value at the memory address constituted by the page number P and the subaddress derived from the connection identifier CI and time stamp TSTP provided at its inputs to 0.

In this way a memory location of MU is reset as soon as copies to be registered at that location are no longer expected.

After this reset operation the control unit CU deactivates the reset signal applied to MU via the circuit S/R and changes the value of the signal S' applied to the selection input of the multiplexer MUX2. As a consequence MUX2 passes to its outputs the signals applied to its inputs by the header processing unit HPU.

The control unit CU in this way constitutes clearing means of the filtering unit.

In the following it is described how to determine the number of pages contained in the memory unit MU, how the header processing unit HPU determines the value of the page number to be passed to the multiplexer MUX2 and to the control unit CU and how the instants and sequence of clearing these pages are determined by the control unit CU.

For this purpose reference is made to the time sequence diagram of Fig. 4, where following symbols are used :

- TSTPIN is the instant at which an initial time stamp TSTPIN is assigned to a packet applied to one of the input ports of the switching network;
- Dmin the minimum time needed to transfer a packet from an input to an output of the network. This transfer time is from now on called transfer delay;
- Dmax the maximum transfer delay of a packet through the network;
- TSTPmax is the time interval starting at the assignment of an initial time stamp value, after which the maximum time stamp value is assigned, i.e. at TSTPIN + XxTSTPmax, a wrap-around occurs; where X is an integer value,
- SET is the time interval during which a first copy of a packet can be received; which corresponds to the time interval during which a location of the memory unit MU (Fig. 3) is available for registering a corresponding first copy of a packet.
- RESET is the time interval available to clear a location of the memory unit MU (Fig. 3) where a received first copy of a packet has been registered.

First the number of pages contained in the memory unit MU is determined.

Supposing this number is equal to n, then the time interval RESET available to clear a memory location is equal to n times TSTPmax - (Dmax-Dmin). Indeed, a first copy of a packet applied to an input port at the instant TSTPIN can be received by the corresponding filtering module up to the instant TSTPIN + Dmax to be stored in MU at a memory location of for instance page PAGE 1. A subsequent first copy with a time stamp value different from TSTPIN is registered on the same page PAGE 1 of MU. When, due to wrap around of the time stamp at the time TSTPIN + TSTPmax again a copy with time stap TSTPIN is received, i.e. in the interval TSTPIN + TSTPmax + DMIN TSTPIN + TSTPmax + Dmax, this copy must be registered on a new page, e.g. page PAGE 2. New pages are in this way used until the n th page whereafter page PAGE 1 has to be reused. In other words the location on page PAGE 1 where the first

mentioned copy with time stamp TSTPIN was registered, has to be cleared within the time interval TSTPIN + Dmax, TSTPIN + nxTSTPmax|Dmin as shown in Fig. 4, since from the instant TSTPIN|nxTSTPmax + Dmin on a copy of another packet also with time stamp TSTPIN to be registered on page PAGE 1 can be received. The time interval RESET is consequently equal to (TSTPIN + nxTSTPmax + Dmin)-(TSTPIN + Dmax) i.e. nxTSTPmax-(Dmax + Dmin).

As a consequence the number of pages is equal to

$$\frac{RESET + (Dmax - Dmin)}{TSTPmax}$$

or the integer value thereof plus 1 if the result of the division is fractional. For the considered embodiment this calculation results in 4 pages as shown in Fig. 4, where PAGE 1 to PAGE 4 represent the page with number 1 to 4 respectively.

In the following it is described how the header processing unit HPU determines the value of the page to be used by the memory unit MU for registration of a first copy, i.e. the value of P applied to the address input P of MU.

A first copy of a page packet with time stamp TSTPIN has to be registered on PAGE 1 in the interval TSTPIN + Dmin, TSTPIN + Dmax. A subsequent copy of packet with the same time stamp assigned to it after wrap-around has to be registered on PAGE 2 as explained above. This latter packet arrives in the filtering unit during the interval TSTPIN + TSTPmax + Dmin, TSTPIN + TSTPmax + Dmax . During this latter interval however copies of packets applied to an input port before the wrap-around which have to be registered on page PAGE 1 can still be received by the filtering unit F11. This means that during this interval the signal produced at the output P of the header processing unit HPU (Fig. 3) has either the value PAGE 1 or PAGE 2 depending on the value of the time stamp included in the header of a received copy, i.e. a value before or after wrap-around respectively.

To determine the value of the page provided at the output P, the header processing unit HPU uses a 10 bit counter (not shown) which is synchronous with an 8 bit counter (also not shown) used at the input ports of the network, the latter counter being used to generate the time stamp values inserted in the header of the information packets. This time stamp value wraps around at 256. The 2 most significant bits of the 10 bit outputs of the 10 bit clock indicate the page number of the page to to be used: If the time stamp value of the received copy is smaller than the value of the 8 least significant bits of the 10 bit clock, then the value of the page to be used is equal to the value of the mentioned 2 most significant bits plus 1, otherwise the page value is equal to the value indicated by the latter 2 bits.

Suppose for example that after a first wrap around the 10 bit clock indicates the value 0100000010 and a copy with time stamp 00000001 is received. This time stamp was assigned after wrap around and the corresponding copy has to be registered on page PAGE 2, whilst a copy with for instance time stamp 11111110 assigned before wrap around has to be registered on page PAGE 1.

An explanation is now given of how the instant of clearing the above pages by the control unit CU is determined, the sequence thereof being indicated by the signal P applied to the corresponding input of CU.

As shown in Fig. 4 and explained earlier, a first copy of a packet with time stamp TSTPIN can be received by a filtering module from the instant TSTPIN + Dmin on, whilst the memory location where that copy is registered may be cleared or reset from TSTPIN + Dmax on. This means that the control unit CU of Fig. 3 has to wait for at least an interval Dmax - Dmin after receipt of the above mentioned first copy by the header processing unit HPU before passing the signals P, CI and TSTP applied to its inputs by the latter to the memory unit MU and controlling the set/reset circuit S/R to reset the corresponding memory location. The signal C' applied to the control input of the control unit CU indicates as explained earlier whether the received copy is a a first one or not.

It has to be noted that an information packet can be identified by a sequence number, unique for each connection, instead of by a time stamp, unique for each input port. In that case a similar reasoning as above is applicable.

Based on the functional description of the header processing unit HPU, the control unit CU and the memory unit MU, their realization is obvious for a person skilled in the art and is therefore not described in detail.

It has to be noted that the above described filtering module filters out the first one of a series of copies. Inserting an error check word in the header of the packet before copying it and adding an additional error processing logic in the header processing unit HPU would make it possible to detect errors in transferred copies and to filter out not the first received copy, but the first received copy without errors.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and

not as a limitation on the scope of the invention.

Claims

1. Packet transfer control arrangement to ensure that an information packet transferred from an input to an output of a packet switching network is available in correct form at said output, characterized in that said arrangement includes :
   - copying means (BM, BMMU) at said input to make at least two copies of said information packet,
   - means to transfer said copies independently from each other over said packet switching network to said output;
   - a filtering module (F11/mn) at said output to filter out one copy of said copies and apply it to said output.

2. Packet transfer control arrangement according to claim 1, characterized in that said arrangement also includes routing means (HAA11/mn) which are associated to said copying means and include in said copies routing information to route said copies through said switching network over at least partly separate paths.

3. Packet transfer control arrangement according to claim 1, characterized in that said filtering module includes :
   - a plurality of memory modules;
   - selection means (MPU) to receive said copies, to register the receipt of a first acceptable copy of said copies at a selected location of a selected one of said memory modules and to discard any other copy;
   - clearing means (CU) to clear said selected location after a predetermined time interval starting at the receipt of a first one of said copies, said selected location being then again available;

   said plurality of memory modules being determined at least by the transfer time of said copies over said network and the time needed by said clearing means to clear said selected location.

4. Packet traffic control arrangement according to claim 3, characterized in that said packet and the copies thereof include a packet identifier (TSTP) and a connection identifier (CI) identifying the communication to which said packet belongs, said packet identifier (TSTP) together with said connection identifier (CI) determining said selected location.

5. Packet traffic control arrangement according to claims 4 and 5, characterized in that the values of said packet identifier (TSTP) wraps around at a predetermined maximum value, the interval between assignment of an initial value of said packet identifier and assignment of said maximum value thereof also determining said plurality of memory modules, and the instant of said wrap around determining said selected memory module.

6. Packet transfer control arrangement according to claim 2, characterized in that said routing means determine said routing information based on routing tables included in switching nodes included in said packet switching network, the content of said routing tables depending on the structure of said packet switching network and on a predetermined reliability of elements of said packet switching network.

7. Packet transfer control arrangement acording to claim 1, characterized in that said copying means include means to insert error check data in said copies and that said filtering means include detection means to detect corrupted copies based on said error check data.

8. Filtering module for filtering one copy of a packet of information out of at least two copies of said packet, said copies being transferred from an input to an output of a packet switching network, characterized in that said module includes:
   - a plurality of memory modules;
   - selection means (MPU) to receive said copies, to register the receipt of a first acceptable copy of said copies at a selected locaiton of a selected one of said memory modules and to discard any other copy;
   - clearing means (CU) to clear said selected location after a predetermined time interval starting at the receipt of a first one of said copies, said selected location then being again available;

   said plurality of memory modules being determined at least by the transfer time of said copies over said network and the time needed by said clearing means to clear said selected location.

9. Method for ensuring that an information packet transferred from an input to an output of a packet switching network is available in correct form at said output, characterized in that said method includes, for each packet to be protected, the steps of :

- making at least two copies of said packet;
- transferring said copies over said network to said output; and
- filtering at said output one acceptable copy out of said copies.

10. Method according to claim 5, characterized in that said copies are transferred over said network in such a way that they follow paths which are at least partly separate.

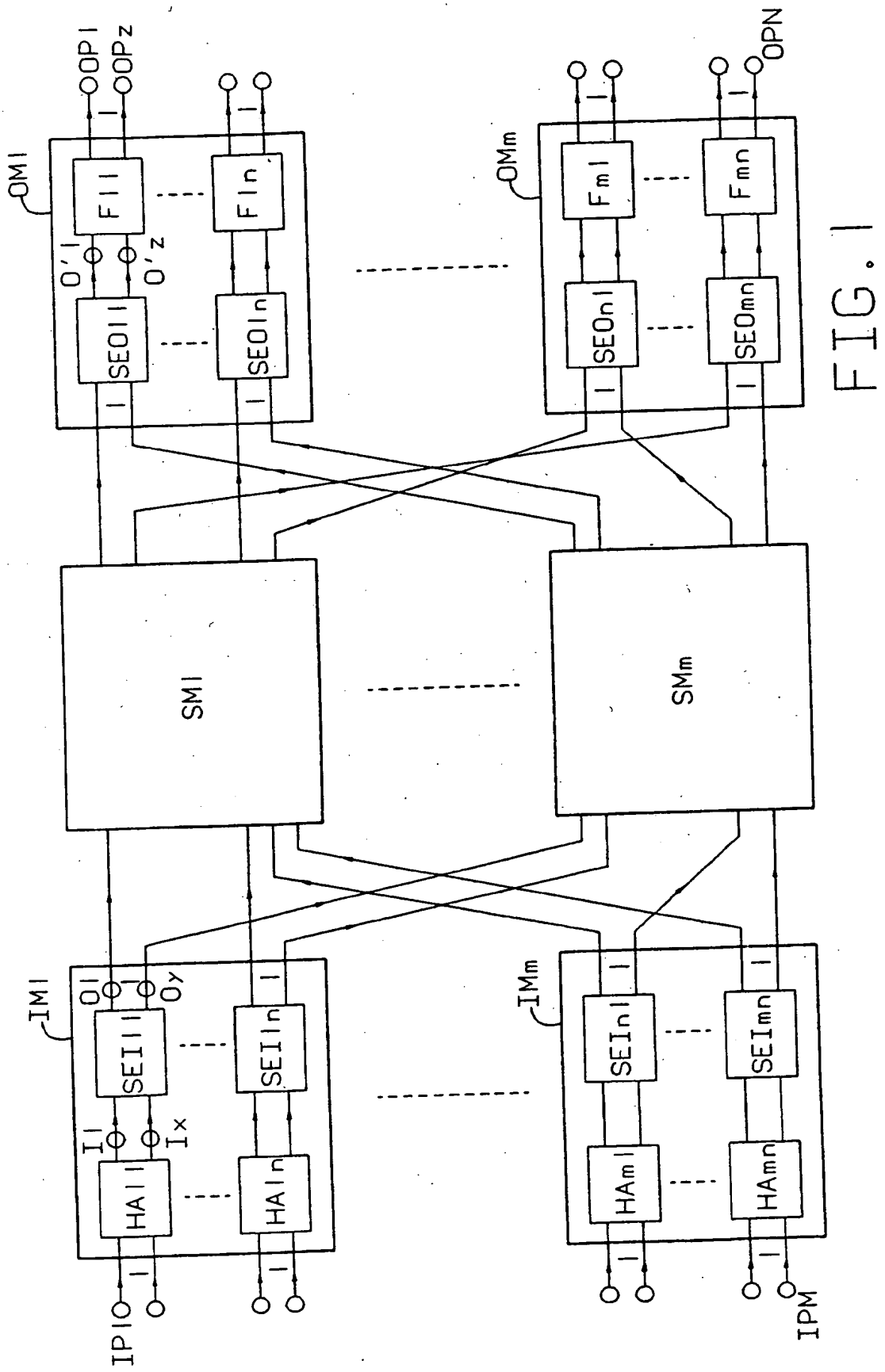

FIG. 1

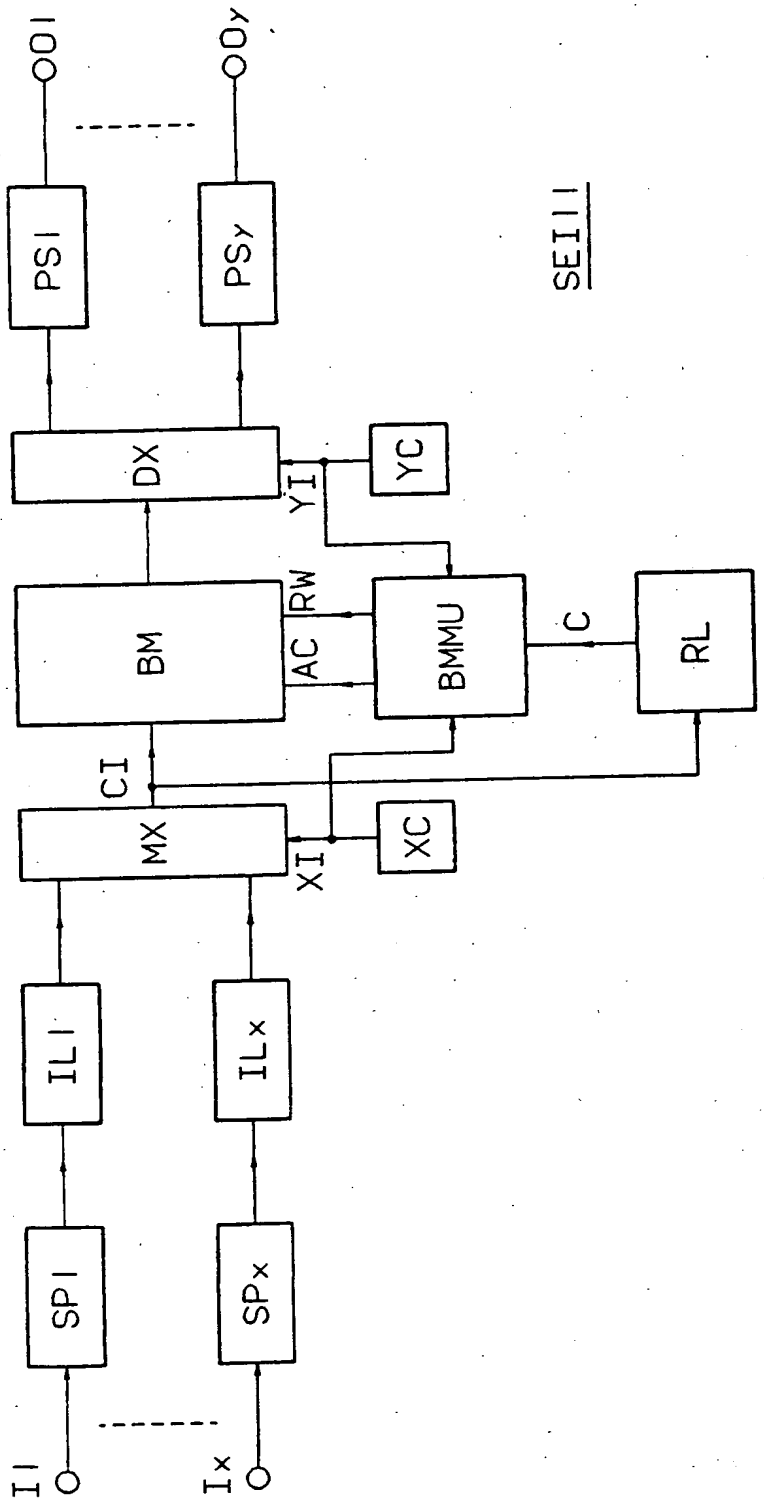

FIG.2

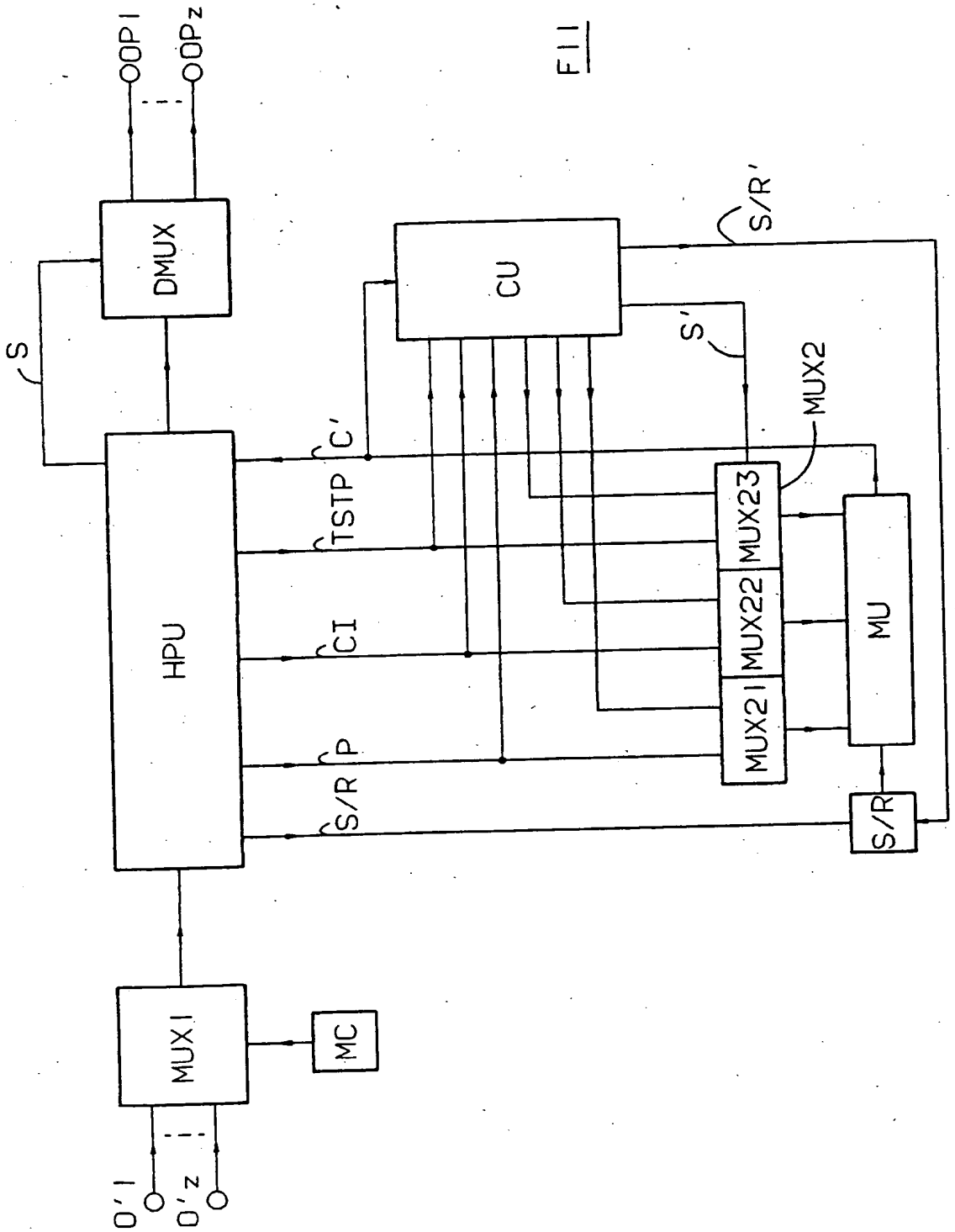

FIG.3

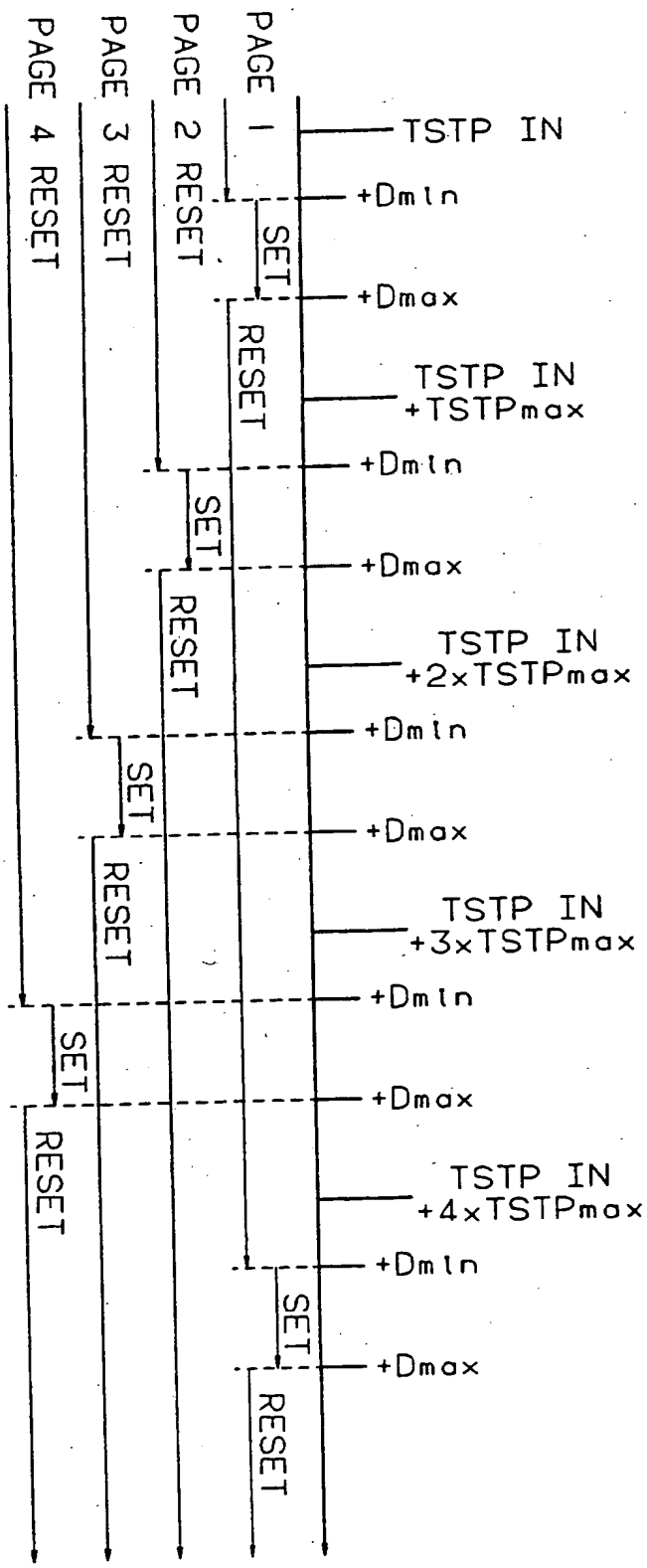

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 20 2660

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 5)
X	EP-A-0 384 936 (SIEMENS AG) * Column 3, lines 1-20; column 4, line 10 - column 5, line 47; column 6, line 13 - column 8, line 24; column 9, lines 17-27 *	1,2,6,7,9,10	H 04 L 12/56
A	---	3-5	
A	GB-A-2 165 124 (ATT) * Abstract; page 2, lines 6-12 *	2,6	
	-----		TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H 04 L

~~The present search report has been drawn up for all claims~~

Place of search	Date of completion of the search	Examiner
THE HAGUE	30-01-1992	ALI A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

European Patent Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid,

namely claims:

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions,
namely:

see sheet -B-

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid,

namely claims:

☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims,

namely claims: 1-7,9,10

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-7,9,10 : Packet transfer control arrangement and method.

2. Claim 8 : Filtering module.